Abstract of the Disclosure

Clock and data recovery circuitry is provided that is used in integrated circuits such as programmable logic device integrated circuits. The clock and data recovery circuitry may recover digital data and an embedded clock from a high-speed differential input data stream. The clock and data recovery circuitry may have automatic mode switching capabilities. When operated in reference mode, the clock and data recovery circuit may use a first phase-locked loop to lock onto a reference clock. When operated in data mode, the clock and data recovery circuit may use a second phase-locked loop to lock onto the phase of the differential data stream. A control circuit may automatically switch the clock and data recovery circuit between the reference mode and the data mode. Override signals may be used to force the clock and data recovery circuit out of the automatic mode and into either the reference or data mode.